REMARKS/ARGUMENTS

The office action of March 26, 2004 has been carefully reviewed and these remarks are responsive thereto. Reconsideration and allowance of the instant application are respectfully requested. Claims 28-70 remain in this application. Claims 1-27 were previously canceled without prejudice or disclaimer and new claims 71-73 have been added.

Claims 28-70 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. patent no. 5,059,815 to Bill et al. ("Bill") in view of U.S. patent no. 5,734,290 to Chang et al. ("Chang") and Applicant's admitted prior art figure 1.

Independent claims 28, 42 and 56 are directed to a voltage generating/transferring circuit. As amended, each of claims 28, 42 and 56, calls for, among other features, a third transistor connected to an output node, being unconnected to a gate of a first transistor, wherein when the third transistor transfers a second voltage from a source of the third transistor to a drain of the third transistor, the voltage generating/transferring circuit becomes disabled, and as long as the third transistor transfers the second voltage, the third transistor is on.

According to an illustrative implementation of the invention of claims 28, 42, and 56, if the third transistor is ON when the voltage generating/transferring circuit is disabled, the voltage of the output node connected to the third transistor can be set at a fixed level, thereby preventing malfunction of the voltage generating/transferring circuit.

To show the third transistor recited in claims 28, 42 and 56, the action relies on N channel MOS transistor 340 in Fig. 3 of Bill. Notably, the gate and drain of transistors 320, 330 and 340 of Bill do not function as switches since each is set to a Vcc (power supply voltage) level. Rather, the gate and drain of each transistor merely charges the source of the respective transistor to a potential level falling within the range of Vcc-Vt (Vt represents the threshold voltage of the MOS transistor). Thus, if the output node of the Fig. 3 circuit (allegedly a voltage transferring circuit) of Bill is set at a level beyond the range of Vcc-Vt when the circuit is disabled, transistors 320, 330 and 340 are turned OFF, and the output node is switched to the floating state. Consequently, the circuit can malfunction easily. In view of the foregoing, Bill does not teach or suggest a voltage transferring circuit as recited in claims 28, 42 and 56 including a third transistor connected to an output node, being unconnected to a gate of a first

transistor, wherein when the third transistor transfers a second voltage from a source of the third transistor to a drain of the third transistor, the voltage generating/transferring circuit becomes disabled, and as long as the third transistor transfers the second voltage, the third transistor is on.

Neither Chang nor Fig. 1 of the instant application overcome the aforementioned deficiencies noted with respect to Bill. Therefore, even assuming, but not admitting, that the combination of Bill, Chang and Fig. 1 of the instant application is proper, that combination does not result in the inventions of claims 28, 42 and 56. Claims 29-41, which ultimately depend from claim 28, claims 43-55, which ultimately depend from claim 42, and claims 57-70, which ultimately depend from claim 56, are patentably distinct over the applied combination for the same reasons as their ultimate base claim and further in view of the additional advantageous features recited therein.

New claims 70-73 are fully supported by the specification and are believed allowable over the cited art alone or in combination.

CONCLUSION

If any additional fees are required or if an overpayment is made, the Commissioner is authorized to debit or credit our Deposit Account No. 19-0733, accordingly.

All rejections having been addressed, applicant respectfully submits that the instant application is in condition for allowance, and respectfully solicits prompt notification of the same.

Respectfully submitted,
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